FIG. 1 PRIOR ART

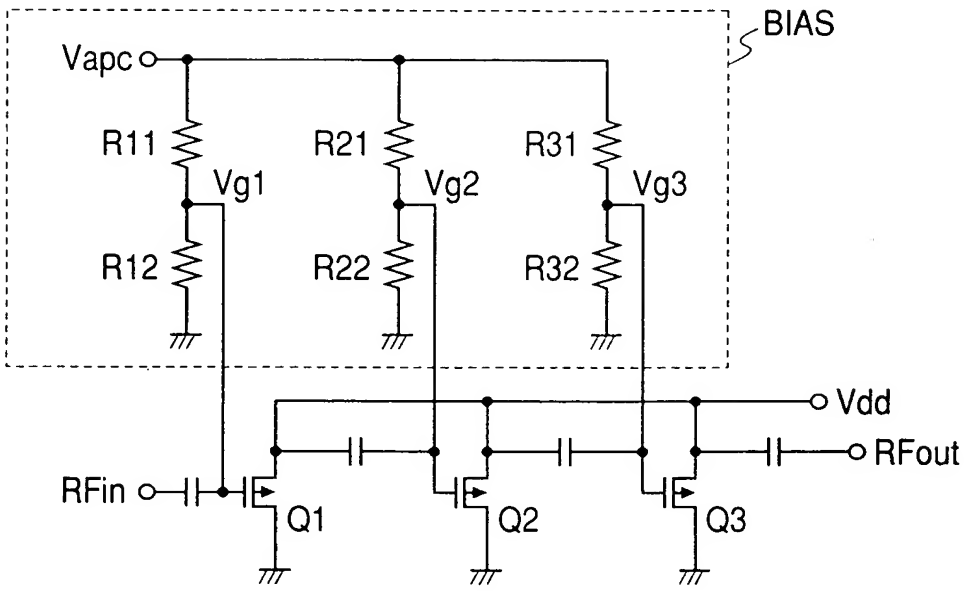


FIG. 2 PRIOR ART

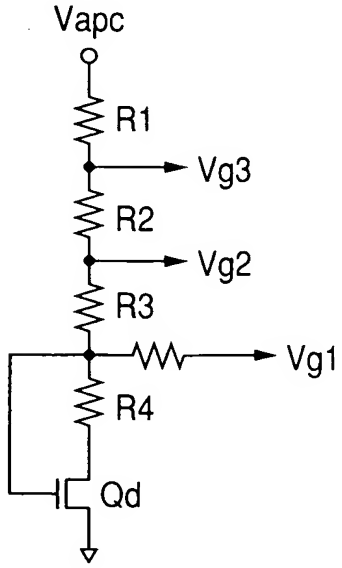


FIG. 3

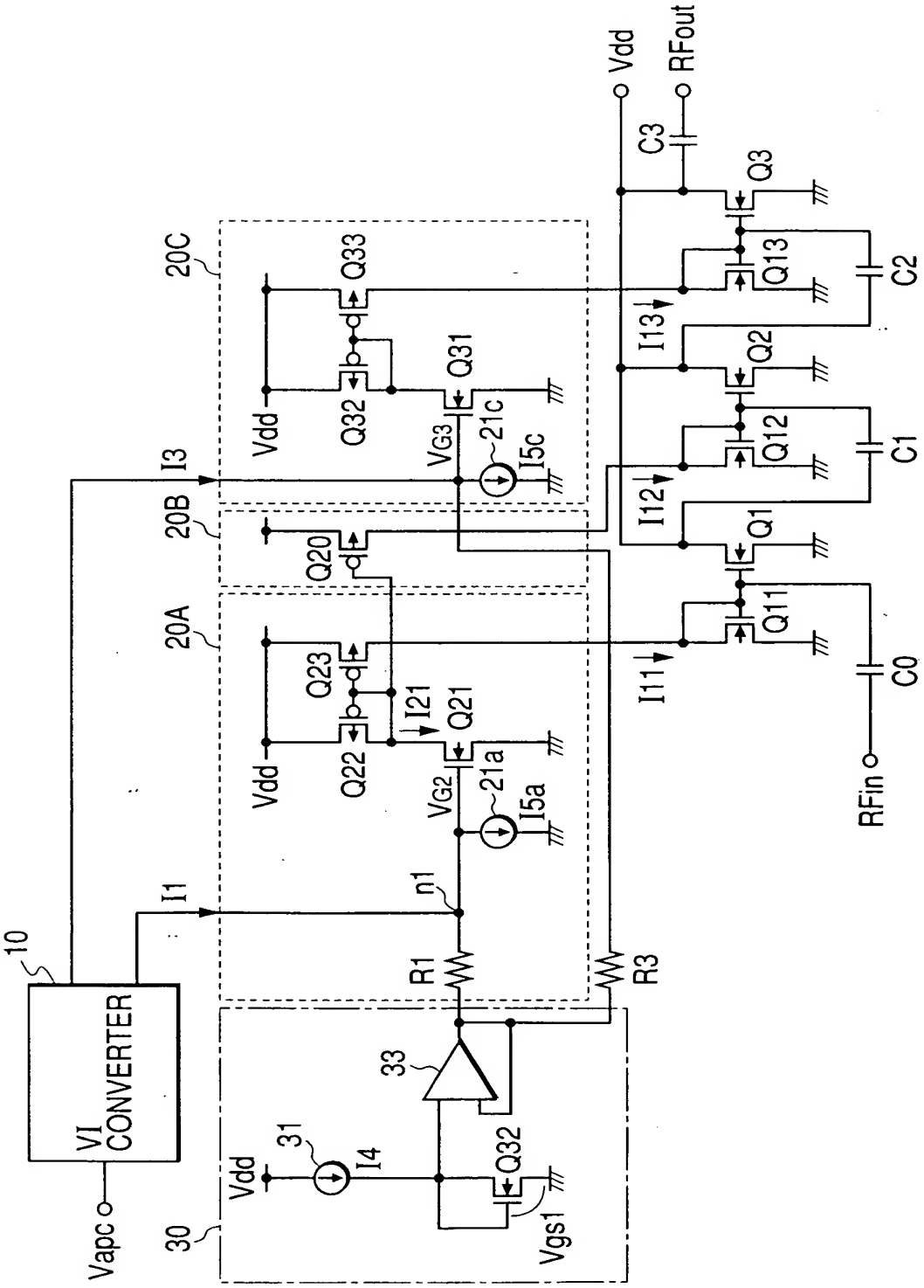

Vdd
RFout
C3
Q3
Q13
C2
I13
Q2
Q12
C1
I12
Q1
Q11
C0
I11
RFin
20C
Q33
Q32
Q31
21c
I5c
VG3
I3
20B
Q20
20A
Q23
Q22
I21
Q21
21a
I5a
VG2
n1
I1
10
VI CONVERTER
Vapc
R1
R3
33
31
I4
Q32
Vgs1
30

FIG. 4

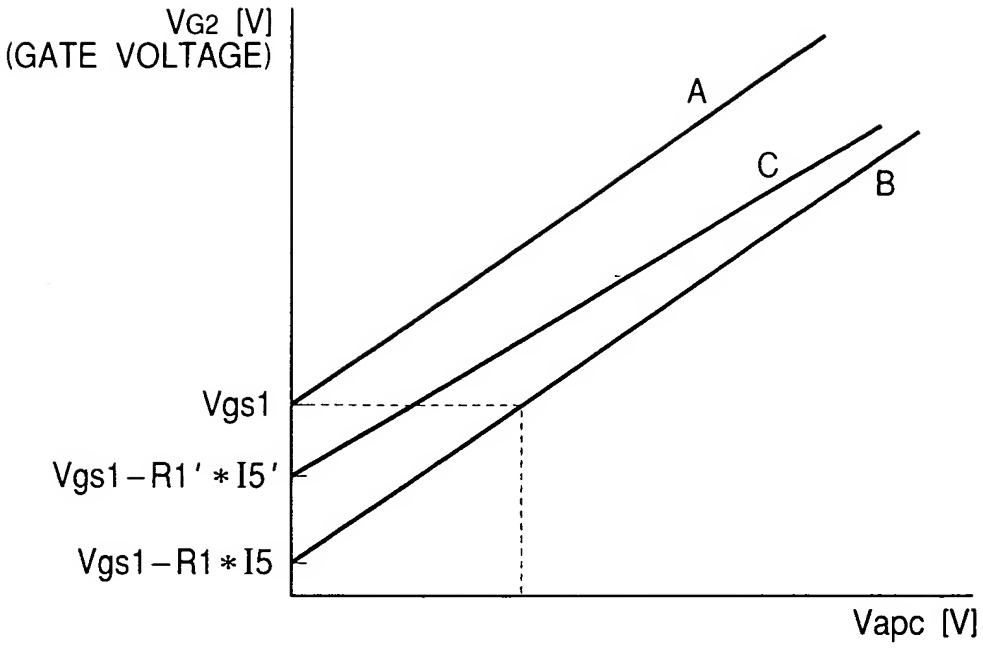

VG2 [V]
(GATE VOLTAGE)
A
C
B
Vgs1
Vgs1−R1′∗I5′
Vgs1−R1∗I5
Vapc [V]

FIG. 5

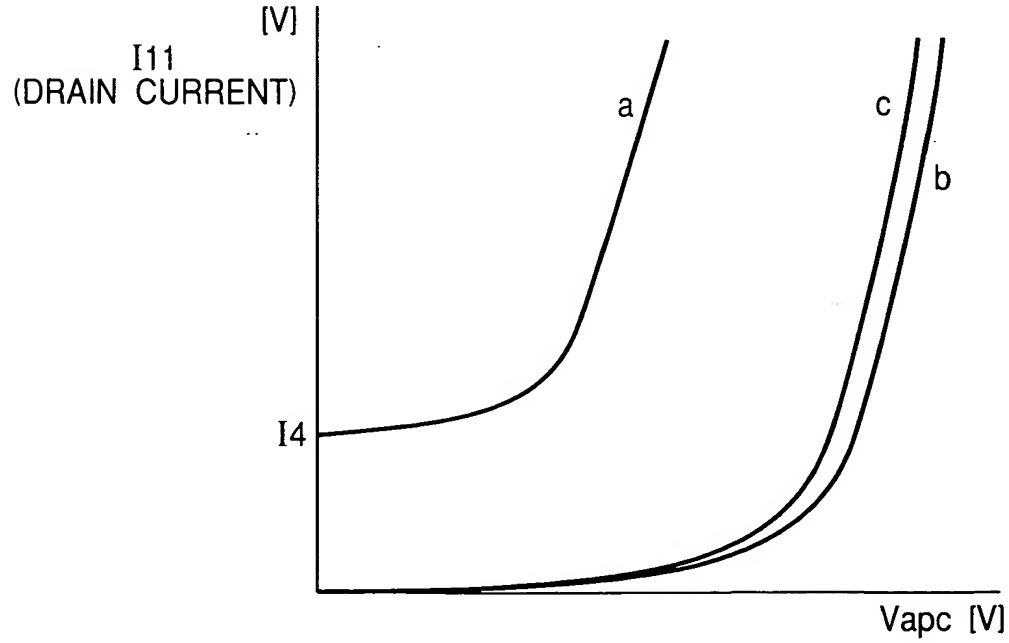

[V]
I11
(DRAIN CURRENT)
a
c
b
I4
Vapc [V]

FIG. 6

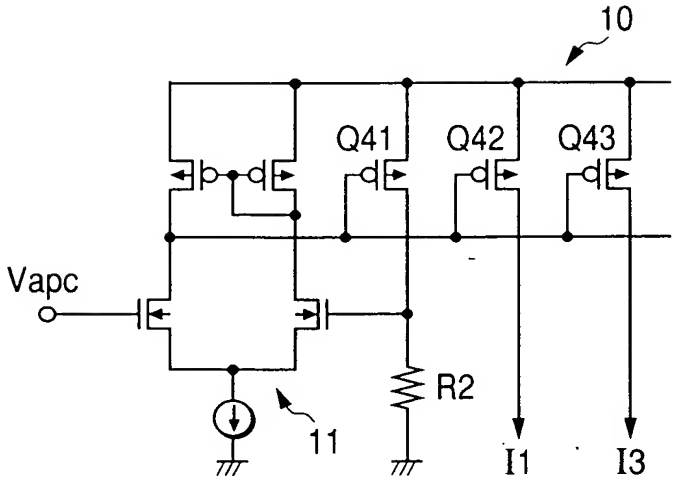

10
Q41
Q42
Q43
Vapc
R2
11
I1
I3

FIG. 7

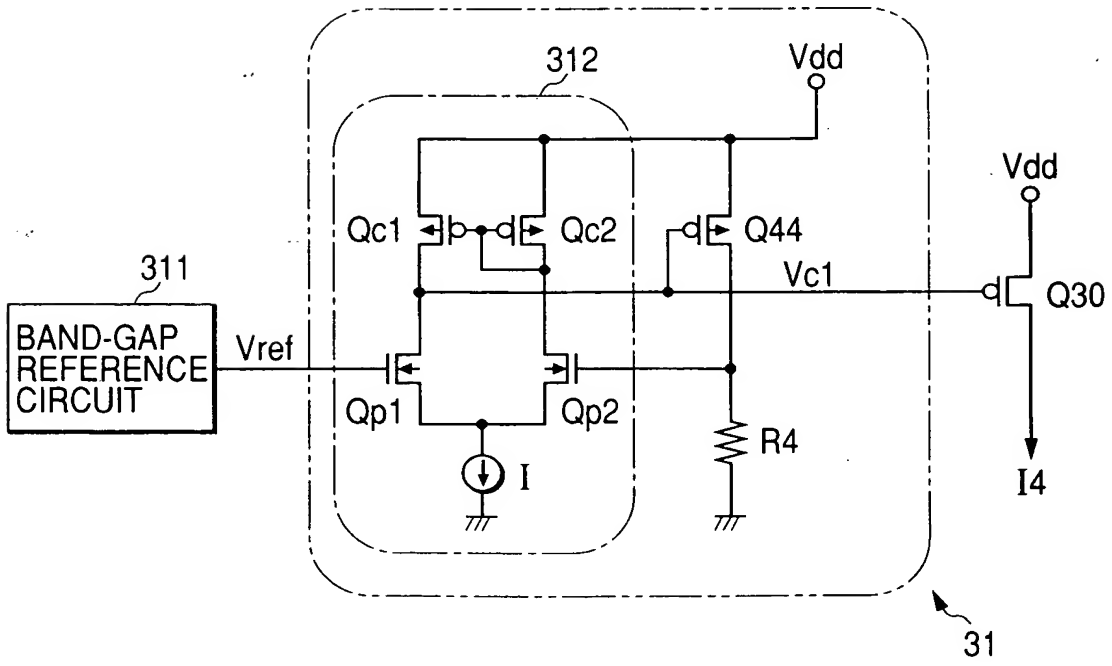

312
Vdd
Vdd
Qc1
Qc2
Q44
311
Vc1
Q30
BAND-GAP
REFERENCE
CIRCUIT
Vref
Qp1
Qp2
R4
I
I4
31

FIG. 8

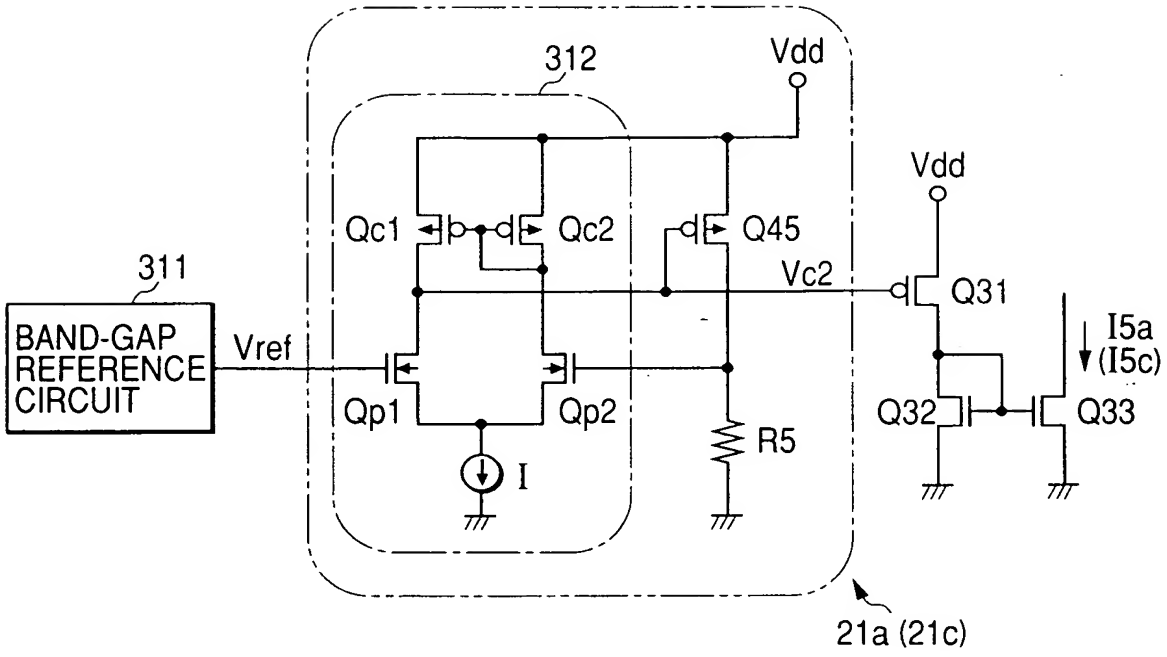

312
Vdd
Vdd
Qc1
Qc2
Q45
311
Vc2
Q31
BAND-GAP
REFERENCE
CIRCUIT
Vref
I5a
(I5c)
Qp1
Qp2
Q32
Q33
R5
I
21a (21c)

FIG. 9

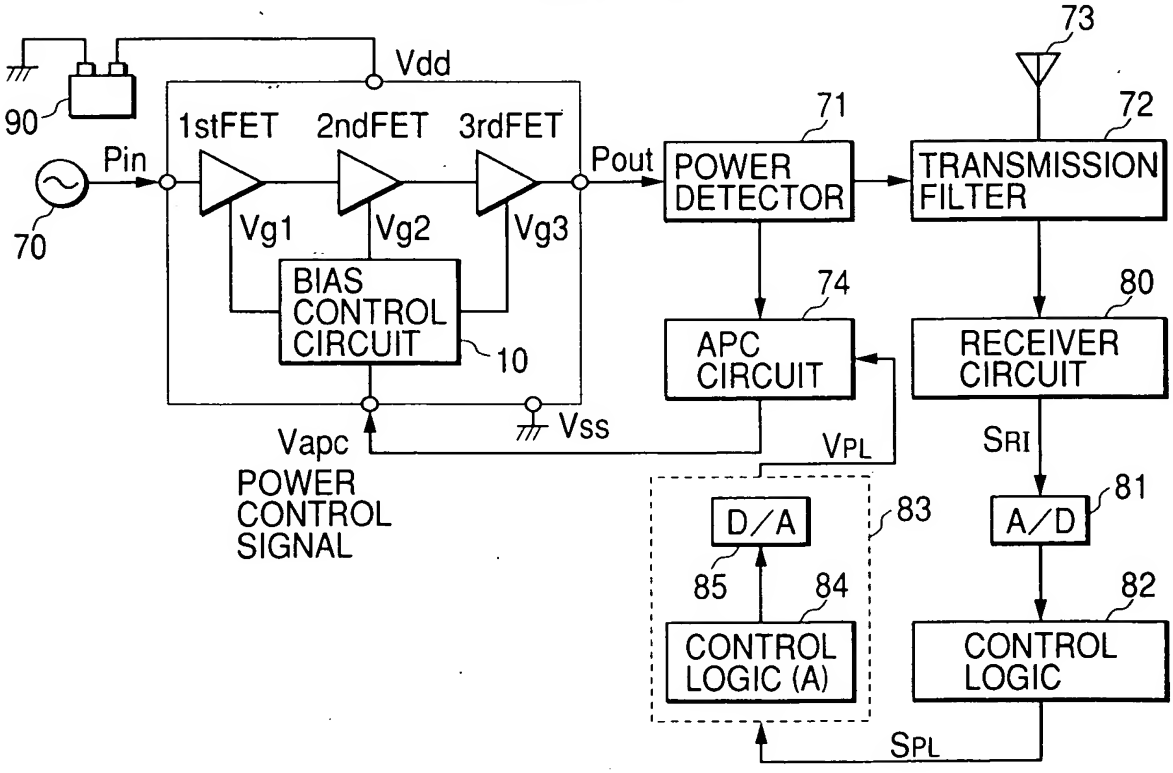
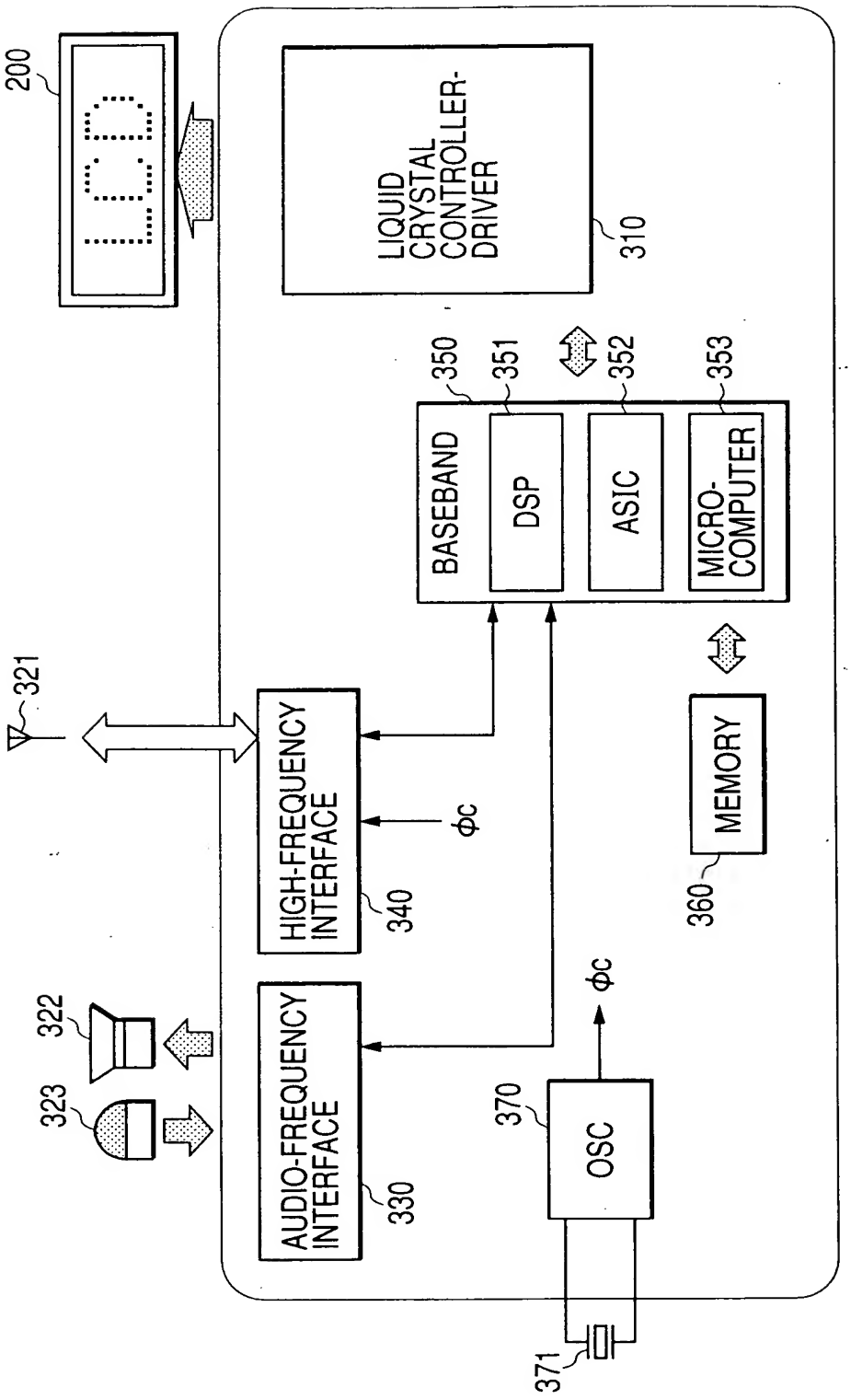

73
Vdd
90
1stFET
2ndFET
3rdFET
71
72
Pin
Pout
POWER
DETECTOR
TRANSMISSION
FILTER
70
Vg1
Vg2
Vg3
74
80
BIAS
CONTROL
CIRCUIT
10
APC
CIRCUIT
RECEIVER
CIRCUIT
Vapc
Vss
VPL
SRI
POWER
CONTROL
SIGNAL
D/A
83
A/D
81
85
84
82
CONTROL
LOGIC (A)
CONTROL
LOGIC
SPL

FIG. 10


200
LIQUID CRYSTAL CONTROLLER-DRIVER
310
350
351
352
353
BASEBAND
DSP
ASIC
MICRO-COMPUTER
321
HIGH-FREQUENCY INTERFACE
340
φc
MEMORY
360
322
323
AUDIO-FREQUENCY INTERFACE
330
370
OSC
φc
371